JFET Basics

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Introduction

A junction field-effect transistor (JFET) consists of a semiconducting channel whose conductance is controlled by an electric field. The terminals at either end of the channel are called source (S) and drain (D). The control electrode that applies the electric field is called the gate (G) and is made of the opposite type of semiconductor material than the channel. Thus, there is a PN junction between the gate and the channel. This PN junction is always reverse biased in normal operation. Figure 1 shows the basic structure.

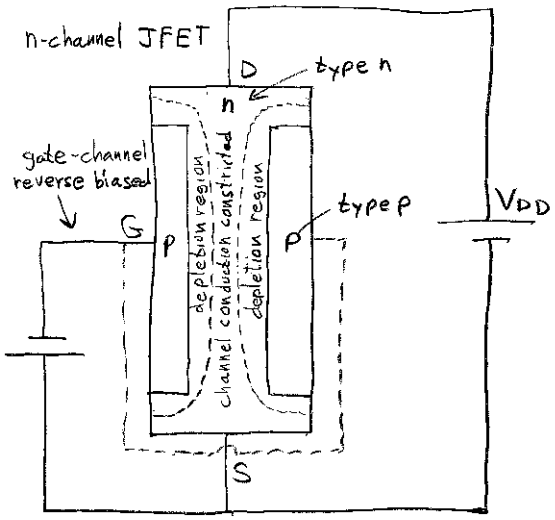

Figure 1: JFET construction and conduction channel controlled by depletion zone

JFETs are known as depletion mode devices because the channel conducts with zero bias voltage applied (i.e. the depletion region has zero width). Applying a reverse bias increases the width of the depletion region which in turn reduces the conduction of the channel. This is the basis for making an amplifier. The channel conduction resembles a resistor for low voltage drops (ohmic region) and becomes a constant current for higher voltage drops (saturation region). The mathematical models we use are based on the saturation region and will provide incorrect results if used in the ohmic region. The model for a field effect transistor is a voltage controlled current source. Many JFETs are so symmetrical in their construction that it makes little if any difference if the source and drain terminals are swapped.

There are two channel types of JFETs. One type is n-channel and the other type is p-channel. Both types operate exactly the same way but the terminal voltages and currents are inverted. This discussion is for n-channel devices.

JFET Basics

The main feature of JFETs is extremely high input resistance – usually at least several hundred megohms. This feature enables the power gain of a JFET amplifier to be huge.

Development of analytic equations for JFET bias condition

The following discussion is about n-channel JFETs. p-channel JFETs operate the same way except that the polarity of the terminal voltages and currents is inverted. There are two parameters that describe the operation of a JFET:

I_{DSS} is the drain saturation current at $V_{GS} = 0$.

V_P is the gate-source voltage, V_{GS}, that causes the channel conduction to drop to zero (actually, the drain current does not go all the way to zero but ceases to decrease below a very small current).

I_{DSS} and V_P have a rough proportional relationship. A high I_{DSS} generally has a higher magnitude V_P. However, because the relationship is dependent on the manufacturing geometry of the JFET there is not a singular proportionality constant. The interpretation of this is that for the spread of I_{DSS} and V_P provided on the data sheet for a specific part that low values of one parameter tend to correlate with low values of the other parameter with the same holding true for higher values. Some data sheets show a typical plot of this relationship.

The drain current is zero when $V_{GS} = V_P$ and is I_{DSS} when $V_{GS} = 0$. The relationship in the saturation region follows a square law as shown in Equation 1. For normal operation, V_{GS} is biased to be somewhere between V_P and 0. Equation 1 gives the approximate drain current, I_D, for a given bias point. This approximation is generally good to within about ten percent and is the accepted equation for all JFET calculations. The more exact model is discussed later.

$$I_D = I_{DSS} * [1 - (V_{GS}/V_P)]^2 \qquad \text{Eq. 1}$$

Equation 1 is valid only if the JFET is operating such that V_{GS} is between 0 and V_P and that V_{DS} is greater than $(V_{GS} - V_P)$, i.e. the saturation region. Note that the drain current, I_D, will be between 0 and I_{DSS}. Figure 2 illustrates an example transfer function for a JFET that has an I_{DSS} of 12 mA and a V_P of -6 volts. The drain current will be less if the transistor is operating in the ohmic region. Although the transfer curve continues into the positive bias region we do not normally operate the JFET there except for very small signals.

Figure 2: Transfer Curve of a Typical JFET showing I_D versus V_{GS}

Figure 3 shows the family curves for a typical JFET. For amplifiers we normally operate the JFET in the saturation region to the right of the dotted parabola curve that separates the ohmic region from the saturation region. Note that that the dotted curve is the solution to $V_{DS} = (V_{GS} - V_P)$. In the ohmic region the device acts similarly to a voltage controlled resistor and in the saturation region the device acts as a voltage controlled current source. The slight tilt of the lines in the saturation region is an extension of the model that includes the effective shunt resistance of the current source. That model is not discussed here. All of the mathematics developed later assumes these lines are perfectly horizontal. It should be noted that for V_{DS} near zero volts (within plus or minus a few tenths of a volt at most) the channel acts as a voltage variable resistor that is linear with voltage. This useful effect continues through zero for small negative voltages across the channel.

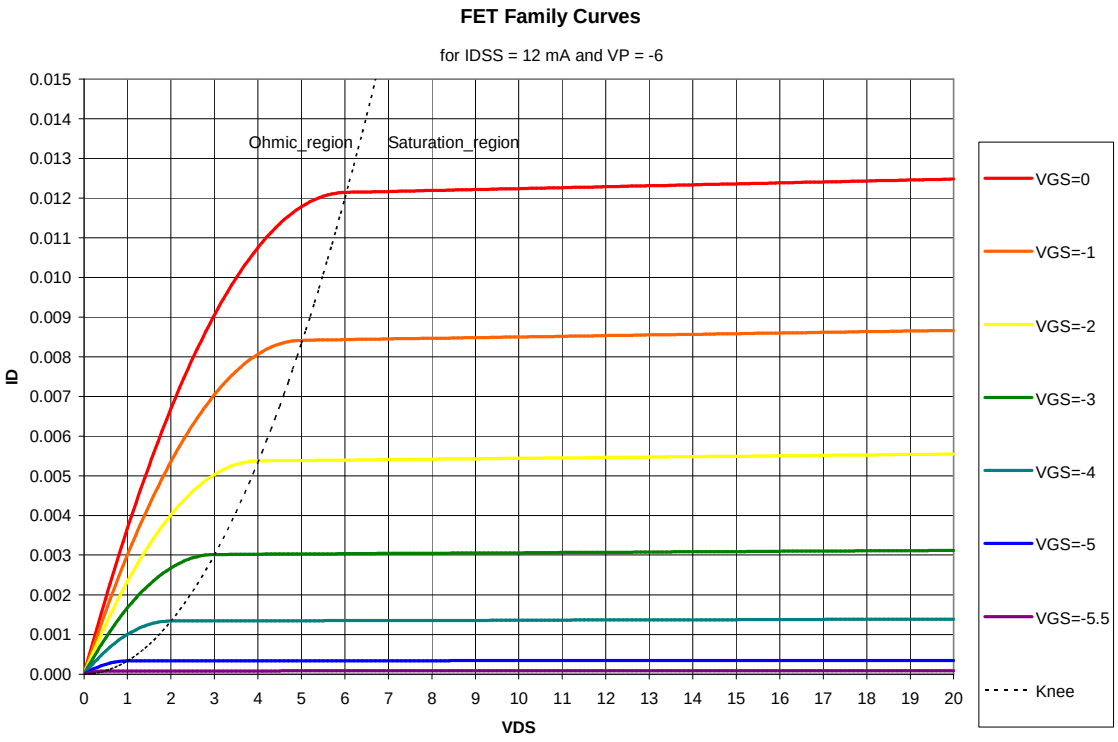

Figure 3: FET Family Curves
Note: V_{GS} is negative – the minus sign may not show on some systems

It is desirable to have the solution to every possible permutation of knowns. The next task is to solve Equation 1 for V_{GS} if I_D is known. This is an exercise for the student but the result is:

$$V_{GS} = V_P * [1 - \text{sqrt}(I_D/I_{DSS})] \qquad \text{Eq. 2}$$

Equations 1 and 2 tell us about the DC bias point operation of the JFET for any combination of knowns.

Development of gain equations for the JFET

Since the JFET is a voltage controlled current source, the gain is the change in drain current divided by the change in gate voltage. This is called the transconductance gain (abbreviated as g_m) of the JFET and has units of conductance which is measured in Siemens. The gain value is very low (typically between 0.0001 and 0.02 – but remember that what matters is power gain and that is very high for a JFET) and is often expressed in mS. The gain is found by taking the derivative of Equation 1 with respect to V_{GS}.

$$g_m = |2 * (I_{DSS}/V_P) * [1 - (V_{GS}/V_P)]| \qquad \text{Eq. 3}$$

The absolute value is used because g_m is always positive. This is done because sign information is lost when terms are squared as in Equation 1. The ratio, I_{DSS}/V_P, will always be negative since V_P is negative for n-channel JFETS and I_{DSS} is negative for p-channel JFETS.

Note from Equation 3 that g_m is a linear function of V_{GS}. When V_{GS} is equal to V_P (i.e. I_D is zero) then g_m is zero. When V_{GS} is equal to zero (i.e. $I_D = I_{DSS}$) then g_m is at the maximum value. The maximum value of g_m is known as g_{mo} and is obtained by setting V_{GS} to zero in Equation 3.

$$g_{mo} = |2 * (I_{DSS}/V_P)| \qquad \text{Eq. 4}$$

At this point it should seem obvious that if high gain is desired then the JFET should be biased as close as practical to I_{DSS}. Equation 4 gives us the ultimate gain possible.

Equation 3 gives us the g_m if V_{GS} is known. For some problems, I_D is known instead. Although V_{GS} can be calculated if I_D is known, it is convenient to have an equation that directly gives us g_m when I_D is known. Simple substitution of Equation 1 into Equation 3 (an exercise for the student) gives:

$$g_m = |2 * \text{sqrt}(I_D * I_{DSS}) / V_P| \qquad \text{Eq. 5}$$

Equation 5 can be expressed in another way that might be convenient for some problems

$$g_m = g_{mo} * \text{sqrt}(I_D/I_{DSS}) \qquad \text{Eq. 6}$$

All three ways of computing g_m give exactly the same answer. The one to use depends on what the knowns at the moment are. It must be remembered that all of these equations assume the JFET is operating in the saturation region. They do not apply in the ohmic region. The user must always take care in using these equations.

The scale factor of 2 in Equations 3 through 5 is nominal. According to the National Semiconductor FET Handbook (1977), that factor can range from about 1.1 to 2.5 but is typically near 2. Keep in mind that we use a model of a JFET based on a simplified quadratic equation.

Equations 1 and 2 can be expressed in a normalized form as

$$I_D/I_{DSS} = [1 - (V_{GS}/V_P)]^2 \qquad \text{Eq. 7}$$

$$V_{GS}/V_P = 1 - \text{sqrt}(I_D/I_{DSS}) \qquad \text{Eq. 8}$$

An equation for the normalized g_m can be developed by dividing Equation 3 by Equation 4 producing

$$g_m/g_{mo} = 1 - V_{GS}/V_P \qquad \text{Eq. 9}$$

By substituting Equation 8 into Equation 9 we can also write

$$g_m/g_{mo} = \text{sqrt}(I_D/I_{DSS}) \qquad \text{Eq. 10}$$

Figure 4 is a plot of Equations 7 and 9. The linear relationship between V_{GS} and g_m is clearly seen. Figure 5 is a plot of Equation 10.

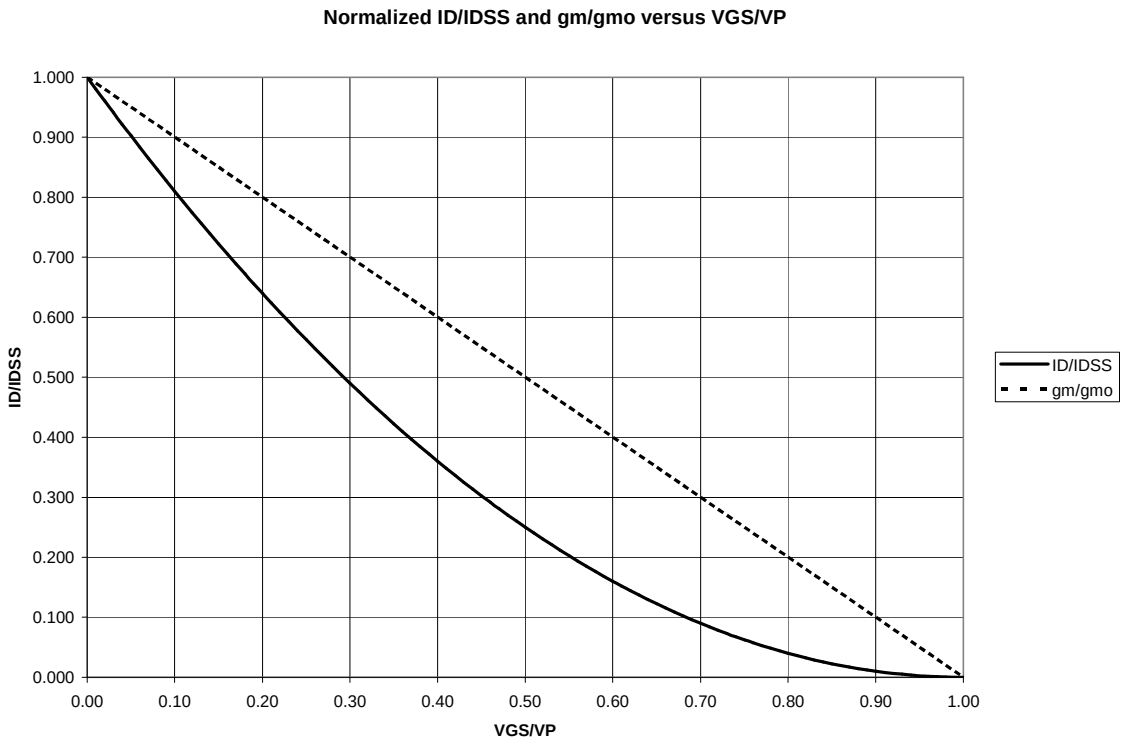

Figure 4: Normalized FET plot

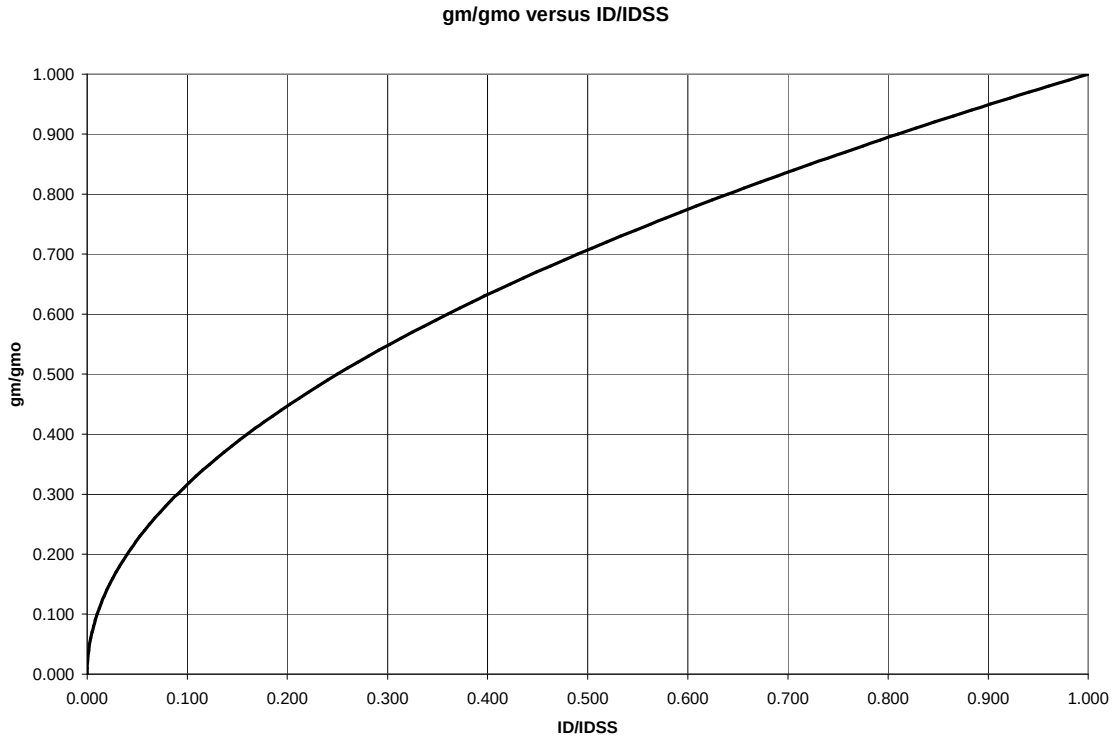

Figure 5: Normalized g_m/g_{mo}

Comparing "Exact" and Approximate JFET Models

In the text, Engineering Electronics, A Practical Approach, by Robert Mauro (copyright 1989 by Prentice-Hall, Inc., Englewood Cliffs, NJ 07632) on pages 209 to 211 there is a development of a more accurate mathematical model for the JFET. The result of that development is:

$$I_D = I_{DSS} * \left[1 - 3 * \left(\frac{V_{GS}}{V_P}\right) + 2 * \left(\frac{V_{GS}}{V_P}\right)^{3/2} \right] \qquad \text{Eq. 11}$$

A commonly used and more convenient approximate model was presented in Equation 1 and is expanded here for comparison:

$$I_D = I_{DSS} * \left[1 - 2 * \left(\frac{V_{GS}}{V_P}\right) + \left(\frac{V_{GS}}{V_P}\right)^{2} \right] \qquad \text{Eq. 12}$$

Figure 6 is a plot of both equations in normalized form. Observe that the error of the approximate model is not very large and that the approximate model predicts a somewhat higher current than the actual. Observe also that the slope of the "exact" curve is steeper thus leading to a higher g_m.

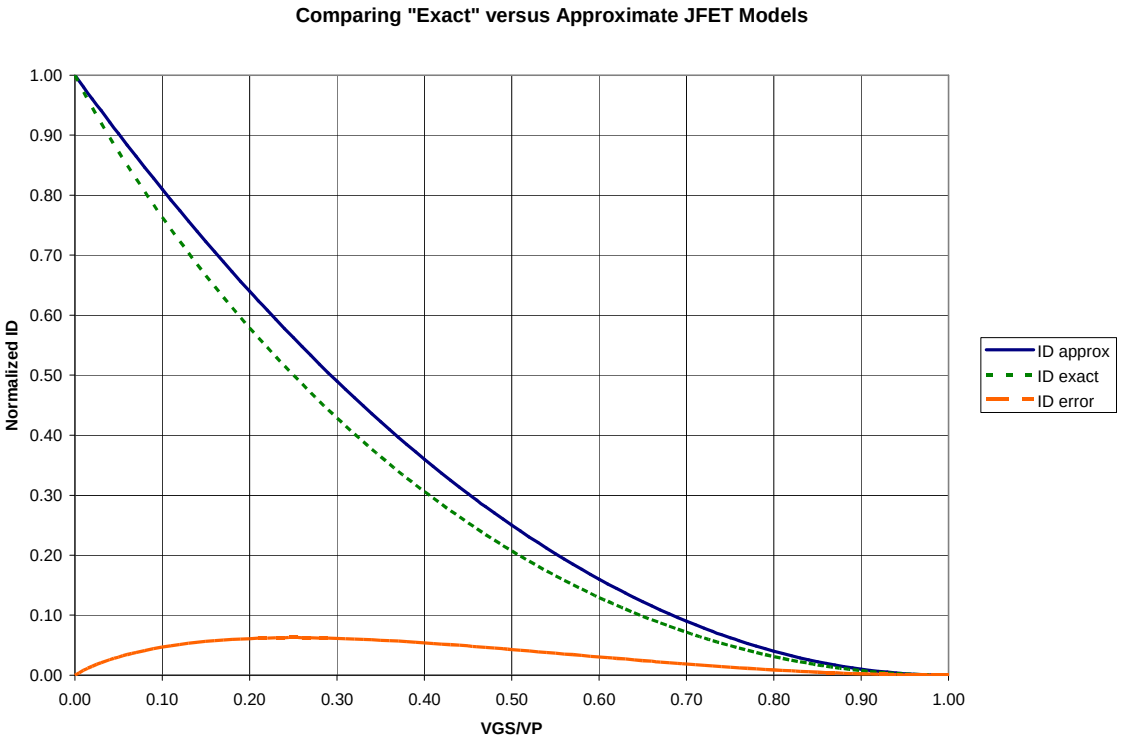

Figure 6: Comparing "Exact" versus Approximate JFET Models

Figure 7 shows the normalized transconductance for both models. Observe that the "exact" model has a higher g_{mo} than the approximate model. This is one reason that on data sheets the stated value of g_{mo} is often higher than what one would calculate using the given I_{DSS} and V_P parameters.

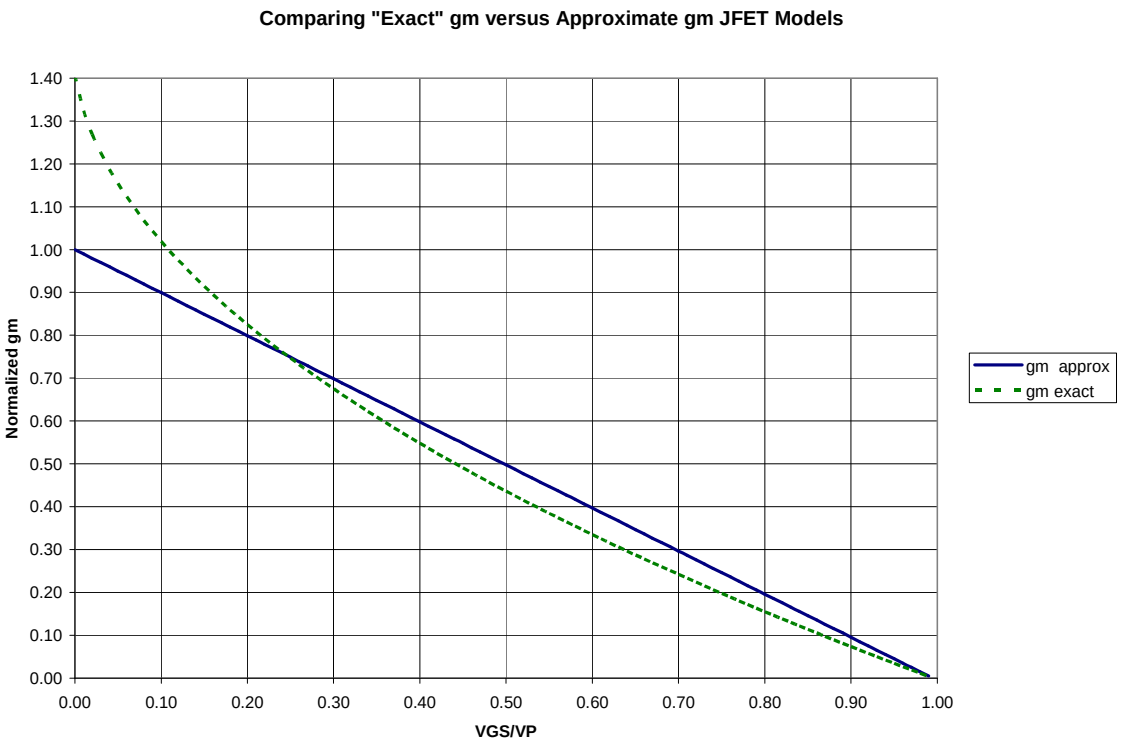

Figure 7: Comparing "Exact" gm versus Approximate gm JFET Models